UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/661,328	09/12/2003	Stephen Alan Cohen	YOR920000333US2	9359

7590 10/13/2004

Alvin J. Riddles
P.O. Box 34
New Fairfield, CT 06812-0034

EXAMINER	
LE, THAO X	
ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 10/13/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/661,328	COHEN ET AL.	
	Examiner	Art Unit	
	Thao X Le	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 September 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *14-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *14-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *09/12/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-13 are cancelled.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 14-15 rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 14 recites the limitation "said body" in line 3, "said conductive member" in line 6, and "said dielectric member" in line 7. There is insufficient antecedent basis for this limitation in the claim.

For the purpose of examination, assuming "said body" is "dielectric body", "said conductive member" is conductive interconnect member" and "dielectric member" is "dielectric body".

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

5. Claims 16-17 are rejected under 35 U.S.C. 102(a) as being anticipated by Applicant Admitted Prior Art (APA).

Regarding claim 16, APA discloses in a process of fabricating sub 250 nanometer size and spacing semiconductor device interconnections wherein conductive interconnect members pass through a portion of a bulk dielectric to a common surface, an improvement comprising the intermediate steps of: depositing a diffusion barrier layer 10, fig. 2, in the formation of conductive interconnect members 2 wherein conductive interconnect members 2 pass through bulk dielectric 1, fig. 2, and then, employing diffusion barrier liner 10 as the conductor for plating in subsequent deposition of metal filling 2 conductive interconnect member 2, specification page 6.

Regarding claim 17, APA discloses the process wherein the material of diffusion barrier liner 10 is a material taken from the group of at least one of Ta, Ti, TaN, TiN, W, and WN, and subsequently deposited metal is copper, fig. 2.

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 14-17 are rejected under 35 U.S.C. 102(b) as being anticipated by US 5592024 to Aoyama et al.

Regarding claim 14, Aoyama discloses the process of preventing high electric filed concentration in a surface of a dielectric body at a facetted shaped intersection with sub 250 nm range size and spacing conductive interconnect member in body comprising the step of:

positioning a mask member 510, fig. 31J, column 26 line 45, of material that is hardened relative to the hardness of dielectric body 509 surrounding at least one conductive interconnect member 515, fig. 31J and over at least a portion of dielectric body 509 at a location below surface a distance defined by the beginning of facetted portion (upper portion of layer 515).

With respect to 'the process of preventing high electric filed concentration in a surface of a dielectric body at a facetted shaped intersection with sub 250 nm range size and spacing conductive interconnect member comprising the step of' do not carry weight, MPEP 2129.

With respect to 'a mask member 510 of material that is hardened relative to the hardness of dielectric body 509' is inherent teaching because the nitride layer 510 would be harder than the inter dielectric TEOS layer 509.

Regarding claim 15, Aoyama discloses the process wherein the material of mask 510 is silicon nitride, column 26 line 45.

Regarding claim 16, Aoyama discloses in a process of fabricating sub 250 nanometer size and spacing semiconductor device interconnections wherein conductive interconnect members pass through a portion of a bulk dielectric to a common surface, an improvement comprising the intermediate steps of: depositing a diffusion barrier layer 514, fig. Fig. 31J, in the formation of conductive interconnect members 515 wherein conductive interconnect members 515 pass through bulk dielectric 509, fig. 31J, and then, employing diffusion barrier liner 514 as the conductor for plating, column 27 line 4, in subsequent deposition of metal filling 515 conductive interconnect member 515, fig. 31J.

With respect to 'a process of fabricating sub 250 nanometer size and spacing semiconductor device interconnections wherein conductive interconnect members pass through a portion of a bulk dielectric to a common surface, an improvement comprising the intermediate steps of' does not carry weight, MPEP 2129.

Regarding claim 17, Aoyama discloses the process wherein the material of diffusion barrier liner 514 is a material taken from the group of at least one of Ta, Ti, TaN, TiN, W, and WN, column 26 line 51, and subsequently deposited metal is copper, column 27 line 2.

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

9. Claims 14-17 are rejected under 35 U.S.C. 102(e) as being anticipated by US 6043146 to Watanabe et al.

Regarding claim 14, Watanabe discloses the process of preventing high electric filed concentration in a surface of a dielectric body at a facetted shaped intersection with sub 250 nm range size and spacing conductive interconnect member in dielectric body, comprising the step of: positioning a mask member 166, fig. 4, column 2 line 60, of material that is hardened relative to the hardness of dielectric body 162, column 2 line 60, surrounding at least one conductive interconnect member 42, column 3 line 52, and over at least a portion of dielectric body 162, fig.

4 at a location below surface a distance defined by the beginning of facetted portion (upper portion of layer 42).

With respect to 'the process of preventing high electric filed concentration in a surface of a dielectric body at a facetted shaped intersection with sub 250 nm range size and spacing conductive interconnect member comprising the step of' do not carry weight, MPEP 2129.

With respect to 'a mask member 166 of material that is hardened relative to the hardness of dielectric body 162' is inherent teaching because the nitride layer 166 would be harder than the low k layer 162.

Regarding claim 15, Watanabe discloses the process wherein the material of mask 166 is silicon nitride, column 3 line 37.

Regarding claim 16, Watanabe discloses in a process of fabricating sub 250 nanometer size and spacing semiconductor device interconnections wherein conductive interconnect members pass through a portion of a bulk dielectric to a common surface, an improvement comprising the intermediate steps of: depositing a diffusion barrier layer 32, fig. 4, column 3 line 52, in the formation of conductive interconnect members 42 wherein conductive interconnect members 42 pass through bulk dielectric 162, fig. 2, and then, employing diffusion barrier liner 32 as the conductor for plating, column 3 line 66, in subsequent deposition of metal filling 42 conductive interconnect member 42, fig. 4.

With respect to 'a process of fabricating sub 250 nanometer size and spacing semiconductor device interconnections wherein conductive interconnect members pass through a

portion of a bulk dielectric to a common surface, an improvement comprising the intermediate steps of' does not carry weight, MPEP 2129.

Regarding claim 17, Watanabe discloses the process wherein the material of diffusion barrier liner 32 is a material taken from the group of at least one of Ta, Ti, TaN, TiN, W, and WN, column3 line 55, and subsequently deposited metal is copper, column 3 line 64.

10. Claims 14-17 are rejected under 35 U.S.C. 102(e) as being anticipated by US 6468898 to Usami et al.

Regarding claim 14, Usami discloses the process of preventing high electric filed concentration in a surface of a dielectric body at a facetted shaped intersection with sub 250 nm range size and spacing conductive interconnect member in dielectric body, comprising the step of: positioning a mask member 4, fig. 3A, of material that is hardened relative to the hardness of dielectric body 3, column 8 line 1, surrounding at least one conductive interconnect member 12, fig. 3A and over at least a portion of dielectric body 3, fig. 3A at a location below surface a distance defined by the beginning of facetted portion (upper portion of layer 12), fig. 3A.

With respect to 'the process of preventing high electric filed concentration in a surface of a dielectric body at a facetted shaped intersection with sub 250 nm range size and spacing conductive interconnect member comprising the step of' do not carry weight, MPEP 2129.

With respect to 'a mask member 4 of material that is hardened relative to the hardness of dielectric body 3' is inherent teaching because the P-SiO_2 layer 4 would be harder than the polymer layer 3.

Regarding claim 15,Usami discloses the process wherein the material of mask 4 is silicon oxide, column 8 line 37.

Regarding claim 16, Usami discloses in a process of fabricating sub 250 nanometer size and spacing semiconductor device interconnections wherein conductive interconnect members pass through a portion of a bulk dielectric to a common surface, an improvement comprising the intermediate steps of: depositing a diffusion barrier layer 10, fig. 3A, column 9 line 12, in the formation of conductive interconnect members 12 wherein conductive interconnect members 12 pass through bulk dielectric 2, fig. 3A, and then, employing diffusion barrier liner 10 as the conductor for plating, column 9 line 13, in subsequent deposition of metal filling 12 conductive interconnect member 12, fig. 3A.

With respect to 'a process of fabricating sub 250 nanometer size and spacing semiconductor device interconnections wherein conductive interconnect members pass through a portion of a bulk dielectric to a common surface, an improvement comprising the intermediate steps of' does not carry weight, MPEP 2129.

Regarding claim 17, Watanabe discloses the process wherein the material of diffusion barrier liner 32 is a material taken from the group of at least one of Ta, Ti, TaN, TiN, W, and WN, column 9 line 12, and subsequently deposited metal is copper, column 9 line 13.

Claim Rejections - 35 USC § 103

11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person

having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

12. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

13. Claims 18-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 5592024 to Aoyama et al in view of US 6043146 to Watanabe.

Regarding claim 18, Aoyama discloses in a process of fabricating sub 250 nanometer size and spacing semiconductor device interconnections wherein conductive interconnect members pass through a portion of a bulk dielectric to a common surface, an improvement comprising the intermediate steps of: etching trench and via shape opening out, fig. 31H, of dielectric body 509 through mask layer 510 in a region below surface, lining open with thin electrically conductive diffusion barrier layer 514, fig. 31J, electroplating a thick metal 515, column 27 line 4, and filling opening surface planarizing over coated surface through chemical mechanical operation, column 27 line 18, and removing mask layer 510 in all portion between opening to a depth that establishes a selected dimension of the upper surface of mask 510 below the surface (upper surface of layer 515), fig. 31L.

But, Aoyama does not disclose coating liner layer 514 with a thin metal layer.

However, Aoyama discloses puttering, CVD or plating, column 27 line 4 can form the metal layer 515. In addition, Watanabe reference discloses he metal layer 42 is electroplating comprising a seed layer (thin metal layer) and thick metal layer, column 3 line 64-67. At the time the invention was made; it would have been obvious to one of ordinary skill in the art to use the electroplated teaching of Watanabe with Aoyama's process, because seeding layer is typical in the electroplating process.

Regarding claims 19-21, Aoyama discloses the process wherein the mask layer 510 is silicon nitride, column 26 line 40, wherein the diffusion barrier layer 514 is Ti, TiN, column 26 line 61, wherein thick metal 515 comprises copper, column 27 line 2.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thao X Le whose telephone number is (571) 272-1708. The examiner can normally be reached on M-F from 8:00 AM - 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael M Fahmy can be reached on (571) 272 -1705. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

LONG PHAM
PRIMARY EXAMINER

PHAM
PRIMARY EXAMINER

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Thao X. Le
05 Oct. 2004